CLAIMS

1. Apparatus for testing an integrated circuit, comprising:

Data source for inputting test signals into an integrated circuit being tested;

A plurality of relays selectively connecting the integrated circuit being tested to the apparatus;

Fan out elements receiving data pulses from the integrated circuit being tested and connected to distribute data pulses to a plurality of latches; and

A strobe element associated with each latch thereby enabling each latch to transfer data pulses from its input ports to its output ports.

2. The apparatus of claim 1, wherein testing components each receive unique data pulses from one of the plurality of latches at a fixed time interval from the time at which each latch is enabled to transfer data pulses from its input ports to its output ports, said testing components receiving data pulses at a frequency that is a fraction of the output frequency of the integrated circuit being tested.

3. The circuit network of claim 2, wherein the fraction is equal to the output frequency of the integrated circuit being tested divided by the number of latches in the apparatus.

4. A method of testing an integrated circuit, comprising the acts of:

fanning out data pulses received from an output port of an integrated circuit being tested;

distributing the data pulses to a plurality of latches; and

calibrating a time at which each one of the plurality of latches is enabled;

5. The method of claim 4, wherein a clock signal of the integrated circuit being tested and a clock signal of a tester are synchronized by the method comprising:

measuring the time between initialization of the integrated circuit being tested and detection of a first data pulse at an input port of a selected latch;

calculating the clock frequency of the tested device therefrom, and;

testing the integrated circuit after calibrating and synchronizing steps are performed;

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6. The method of claim 4, wherein a repetitive bit stream with alternating voltage levels is transmitted from the integrated circuit being tested to calibrate a time at which each one of the plurality of latches is enabled.

7. The method of claim 4, wherein edge transitions at the outputs pins of one of the plurality of latches are monitored in succession to calibrate a time at which each one of the plurality of latches is enabled.